In the Claims:

1-24. (canceled)

25. (new) A first-in first-out memory comprising:

A. memory circuitry having word storage slots, each word storage slot containing a same certain number of bits, and having a read pointer address input and a write pointer address input;

B. data read/write circuitry having a parallel port selectively coupled with each word storage slot, a system data path, a control input, and a scan data input/output;

C. control circuitry having a read pointer address output connected with the read pointer address input and a write pointer address output connected with the write pointer address input, the control circuitry having a control output connected with the control input of the data read/write circuitry, and having a scan control output; and

D. scan storage circuitry separate from the memory circuitry, the scan storage circuitry having a serial input, a serial output, a scan data output/input connected with the scan data input/output of the data read/write circuitry, and a control input connected with the scan control output.

26. (new) The memory of claim 25 in which the scan storage circuit is serial shift circuitry having the certain number of bits, so that the serial shift circuitry has the same number of bits as a word storage slot.

27. (new) The memory of claim 25 in which the scan storage circuit is serial shift circuitry having the certain number of bits, so that the serial shift circuitry has the same number of bits as a word storage slot, and the scan input/output is a parallel connection of the certain number of bits from and to the data read/write circuitry.

28. (new) The memory of claim 25 in which the memory circuitry is free of scan circuitry.

29. (new) A process of scan testing a first-in first-out memory having word storage slots, comprising:

A. setting a read pointer and a write pointer to initial addresses of the word storage slots;

B. operating read/write circuitry to read a first word from a word storage slot indicated by the initial read pointer address into scan storage circuitry that is separate from the word storage slots;

C. shifting the scan storage circuitry to shift the first word out of the scan storage circuitry and simultaneously shift a second word into the scan storage circuitry; and

D. operating the read/write circuitry to write the second word from the scan storage circuitry into a word storage slot indicated by the initial write pointer address.

30. (new) The process of claim 29 in which the shifting includes shifting the scan storage circuitry the same number of bits as are contained in each word storage slot.

31. (new) The process of claim 29 including incrementing the read pointer address and the write pointer address and repeating steps B., C., and D.